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**Title of
Invention****THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE
YIELD AND RELIABILITY OF VLSI DESIGNS**

Application Number :

Date :

First Named Applicant: Robert J. Allen

Confirmation Number:

Attorney Docket Number: BUR920030092US1

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/s/

Attorney

Documents being submitted:	Files
us-ids	BUR920030092US1-usidst.xml us-ids.dtd us-ids.xsl
us-request	BUR920030092US1-usrequ.xml us-request.dtd us-request.xsl
us-assignment	BUR920030092US1-usassn.xml us-assignment.xml us-assignment.dtd BUR920030092US1assign1.tif BUR920030092US1assign2.tif
us-fee-sheet	BUR920030092US1-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd
application-body	BUR920030092US1spec-trans.xml us-application-body.xsl application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd BUR920030092US1sheet1of7.tif BUR920030092US1sheet2of7.tif BUR920030092US1sheet3of7.tif BUR920030092US1sheet4of7.tif BUR920030092US1sheet5of7.tif BUR920030092US1sheet6of7.tif BUR920030092US1sheet7of7.tif

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Comments

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